REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated June 20, 2003. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1, 3-5, 9-11 and 23-24 are under consideration in this application. Claims 2 and 22 are being cancelled without prejudice or disclaimer. Claims 1, 3-5, and 9-11 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention. New claims 23-24 are being added to recited other embodiments described in the specification. Claims 6-8 and 12-21 remain withdrawn.

Additional Amendments

The claims are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1, 2, 9-11 and 22 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,091,466 to Kim et al. (hereinafter "Kim"). Claims 3 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of U.S. Patent No. 6,243,146 B1 to Rho et al. (hereinafter "Rho"), and claim 5 was rejected as being unpatentable over Kim in view of U.S. Patent No. 6,001,539 to Lyu et al. (hereinafter "Lyu"). These rejections have been carefully considered, but are most respectfully traversed.

The liquid crystal display device of the invention, as now recited in claim 1 (Embodiment 1), comprises: a first insulating substrate and a second substrate being disposed so that respective main surfaces thereof are opposite to one another; a liquid crystal layer being interposed between the first and second insulating substrates; gate wiring lines being formed on the first insulating substrate and transmitting scanning signals; a gate insulating

film being composed of the first insulating substrate and the gate wiring lines; drain wiring lines being composed of metal films formed on the gate insulating film and transmitting video signals; thin film transistor sections, each of which has a semiconductor layer located at least over a part of the gate wiring layer, a drain electrode composed of a part of the drain wiring line located on said semiconductor layer and a semiconductor contacting layer formed of a part of said semiconductor layer being contacted with the part of the drain wiring lines, a source electrode composed of another metal film formed on said semiconductor layer to be spaced from and opposite to the drain electrode and another semiconductor contacting layer formed of another part of the semiconductor layer being contacted with a lower surface of the another metal film, and a protective film covering the drain wiring lines, the source electrode, and the drain electrode; and pixel electrode sections, each of which has a pixel electrode being contacted with said source electrodes. A planar pattern of each of said semiconductor layers is broader than those of the metal layers of the drain wiring layer, the source electrodes, and the drain electrodes formed thereon, and a planar pattern of each of said semiconductor layers is broader than those of said semiconductor contacting layers. In particular, each of said drain wiring lines ***DL*** is connected to a pad portion (via its terminal section ***DTM*** above the pad portion; Figs. 1 and 5; page 28, second paragraph) which has at least a metal layer ***d1*** formed in the pixel area and a semiconductor layer ***d0*** formed under said metal layer ***d1***, and a planar pattern of said semiconductor layer ***d0*** formed under said metal layer ***d1*** of said pad portion is broader than a planar pattern of said metal layer ***d1*** (***d0>d1***).

As such, the tensile stress of the metal film ***d1*** is canceled by the compressive stress of the semiconductor film ***d0***, thereby preventing disconnection of the drain wiring lines (page 12, lines 3-5).

The invention is also directed to a liquid crystal display device, as now recited in claim 3 (Fig. 14; Embodiment 3: page 42, line 22 to page 44, line 4), comprising: a first insulating substrate and a second insulating substrate disposed to be opposite to the first insulating substrate; a liquid crystal layer being interposed between the first insulating substrate and the second insulating substrate; charges-holding capacitance sections ***Cstg***, each of which has an upper electrode ***PX*** (ITO1), a dielectric film ***GI*** and a lower electrode ***GL***(g1). In particular, said dielectric film ***GI*** is formed between said lower electrode ***GL*** and the upper electrode ***PX*** at each of said charges-holding capacitance sections ***Cstg*** (right side of Fig. 14), and said upper electrode ***PX*** contacts with said dielectric film ***GI*** through a contact hole ***CNS*** provided by perforating a protective film ***PSV*** formed over said dielectric

film ***GI***, and a semiconductor layer ***AS*** provided between said protective film ***PSV*** and said dielectric film ***GI*** is selectively etched to be only around said contact hole ***CNS*** ("*the [island-shaped] a-Si channel film AS [in Figs. 15A-B] is removed from **only** the section of the through-hole CNS [in Fig. 15C]*" Page 44, lines 1-3; Fig. 14; "*Then, the a-Si channel film AS over the charge-holding capacitance Cstg is selectively etched above the gate insulating film GI formed of SiN at the opening CNS with the resist pattern PRES1 being left*" page 45, lines 17-20).

"The a-Si channel film AS underlying the protective film PSV is etched near the outline of the opening CNS of the charge-holding capacitance Cstg, and if the a-Si channel film AS is thick, the a-Si channel film AS is side-etched into the protective film PSV, so that the transparent conductive film ITO1 to be deposited in a later process may be disconnected.... Accordingly, the etched end surfaces of the protective film PSV and the a-Si channel film AS at the through-hole CNS of the charge-holding capacitance Cstg of the pixel electrode PX have good shapes, whereby the transparent conductive film ITO1 of the pixel electrode PX is not disconnected. (page 46, line 24 to page 47, line 15)." In other words, the upper electrode **PX** is formed on the semiconductor layer **AS** (rather than any metal layer) such that no scooping-out phenomenon will occur underneath the contact hole **CNS** as in the prior art (see the attached explaining drawings).

Applicants respectfully contend that Kim fails to teach or suggest the features of (1) the ***d0>d1*** structure of a pad portion under a terminal section of each drain wiring line (claim 1), and (2) a semiconductor layer ***AS*** provided between said protective film ***PSV*** and said dielectric film ***GI*** being selectively etched to be only around said contact hole ***CNS*** (claim 3).

In contrast, regarding the (1) feature, Kim merely discloses a planar pattern of the semiconductor layer broader than those of the metal layers of the drain wiring layer, the source electrodes, and the drain electrodes formed thereon (Figs. 2D-2F), and a planar pattern of each of the semiconductor layers other than the semiconductor contacting layer formed therein is broader than those of the semiconductor contacting layers, but not a metal layer of a pad portion under a terminal section of each drain wiring line. Rho and Lyu fail to compensate for Kim's deficiencies. Lyu merely discloses a protective film of the conventional LCD has a layered structure having organic and inorganic films but does not disclose the pad portion according to the invention.

Regarding the (2) feature, Kim only discloses a conventional LCD device wherein a pixel electrode 41 contacts with the gate insulating film 17 through a second contact hole 81 which is provided by perforating a passivation film 37 and a storage capacitor electrode 51 at

the charges-holding capacitance section. The storage capacitor electrode 51 provided between a protective film and a dielectric film in Kim is a chromium layer (col. 2, lines 35-39), rather than a semiconductor layer being selectively etched to be only around said contact hole. Therefore, Kim suffers from the scooping-out phenomenon occurring underneath the contact hole as in the prior art (see the attached explaining drawings).

Ryo is relied upon by the Examiner to teach forming a pixel electrode to contact with the gate insulting film by perforating a semiconductor layer at the charges-holding capacitance section. However, Ryo merely discloses making thin or removing the portion of the passivation layer on the storage capacitor electrode to increase the storage capacitance, but not a semiconductor layer formed only around the contact hole on said dielectric film. Therefore, Rho fails to compensate for Kim's deficiencies regarding the (2) feature. Similarly, Lyu fails to compensate for Kim's deficiencies.

As such, the present invention as now claimed in independent claims 1 and 3 is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

JOHN C. BROSKY
REGISTRATION NO. 31,002

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